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Low Voltage Lazzaro's WTA with enhanced loop gain

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Abstract: An additional stage for a Low Voltage Lazzaro's Winner Take All (WTA) circuit is introduced. It allows lowering the voltage supply requirements so that it can be functional in fine line CMOS technology. Electrical measurements of a prototype in CMOS 0.5 μm technology verify the operation of the WTA circuit with $V_{DD} = 1.5$ V. Simulations in PSpice and stability issues are presented as well.

Keywords: WTA, low voltage, non-linear circuits

Classification: Integrated circuits

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1 Introduction

A WTA circuit identifies the highest (lowest) value from a set of multiple input analog signals and it is often referred as a Max (Min) circuit. This kind of circuits plays an important role in the development of complex neural networks, fuzzy controllers and nonlinear filters for image processing. The most commonly used current-mode Winner Take All (WTA), referred as Lazzaro's circuit, is shown in Fig. 1 a [1]. This WTA, and other related Rank Order Filters, has been widely used in many fields (image processing, communications, neural networks, etc.). One of the drawbacks of conventional Lazzaro's circuit, from the voltage supply perspective, is the requirement of a minimum supply $V_{DDMIN} > 2V_{GS}+2V_{DSsat}$, if bias circuits are implemented as cascode current sources. Therefore, these circuits are non well-suited for submicron technologies.

In this paper, a compact WTA suitable for low voltage applications and enhanced gain, by adding a gain stage, is obtained. The letter is organized as follows: the operation of the Lazzaro's WTA cell is described in section 2; the proposed circuit is presented in section 3, while simulations and experimental results are shown in section 4. Finally, conclusions are established in section 5.

2 Lazzaro's WTA

Most of conventional linear and nonlinear analog circuits require supply voltages of at least two gate-source drops. State of the art deep submicrometer CMOS technology uses single supply voltages close to 1 V and transistors have a relatively high threshold voltage ($V_T \sim 0.4$ V). Modern technologies are characterized by a low ratio $V_{DD}/V_T < 3$ and circuits requiring a supply of over two gate-source drops can not be used with transistors with nominal V_T operating in saturated mode or they can have very poor performance characteristics (Bandwidth, accuracy, etc.). Low V_T transistors, available in some fine line technologies, can be used to overcome this limitation but they require additional masks and increased production costs.

The compact WTA circuit proposed by Lazzaro [1] is shown in Fig. 1 a. The circuit has current-mode inputs and a common connection, node "x", among all cells. The principle of operation can be explained as follows: for

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two different input currents $I_{in1} = I + \Delta I$ and $I_{in2} = I$; the excess of current in I_{in1} causes a voltage increment of V_1 and "V_x" (the voltage at node x) due to the follower configuration of transistor M_{21}; V_x will rise until I_{in1} is totally sinked through M_{11}. Since transistors share a common gate voltage, this V_x voltage causes M_{12} to sink ΔI more current than I_{in2}, therefore, V_2 will experiment a gradual decrease towards 0 V approximately. This computation eventually produces a winner cell with a voltage V_1 different from zero and V_x following the input with the highest current, while all other follower transistors are turned off.

However, the main drawback of Lazzaro's approach lies on its high supply requirements accuracy and the low speed response, which is mainly due to the high capacitance associated to node "x". Previous efforts to reduce this high voltage requirement have been made. In [2] using SOI technology, an extra complementary source follower stage is introduced in each cell loop; this fact allows the circuit to work as a Loser Take All (LTA) with a reduction on the voltage requirement. Nevertheless, the limited gain ~0.8 of source followers reduces the loop gain of the cell in this approach, so, there is just a marginal improvement on accuracy over the original Lazzaro's circuit.

Moreover, other authors have proposed diverse modifications to improve the speed of the circuit; this is the case of [3], where a hysteresis loop is added and [4], where a common-source configuration stage improves the overall performance of the cell. In recent works, bulk driven techniques [5] and low V_T technologies [6] have been also used in order to lowering the voltage supply requirement.

Despite of the mentioned drawbacks, its simplicity is the reason because of Lazzaro's approach is still used in many applications.

3 Proposed additional stage

In order to reduce the supply requirements, the loop including the two V_{GS} in series, (M_{1i} and M_{2i}) from Fig. 1 a must be modified. The modified version of the circuit, with an additional common gate stage (MCG), is shown in Fig. 1 b. A common gate amplifier composed by the transistor M_{CG} and biased with current I_{bCG} and $V_{MCG} = 1.07$ V, has been introduced for two purposes: First, it allows breaking the loop of the $2V_{GS}$ in series, lowering the voltage requirements and, secondly, it improves the resolution by increasing the open loop gain [7]. In this way, the voltage requirement for the proposed circuit is $V_{DDmin} \approx V_{GS} + 3V_{DSsat}$ and the winner cell open loop gain is increased to a value:

$$A_{OL} = \frac{g_{m_{M2}}}{g_{m_{M2}} + g_{mb_{M2}}} \left(g_{m_{MCG}} r_{o_{MCG}}\right) g_{m_{M1}} r_{o_{M1}} \tag{1}$$

Where, g_m denotes the small-signal gate transconductance, g_{mb} is the small-signal substrate transconductance and r_o is the transistor output resistance. Since output node "y" is the dominant pole, compensation is implemented with a capacitance Cc in order to avoid ringing in the transient response.

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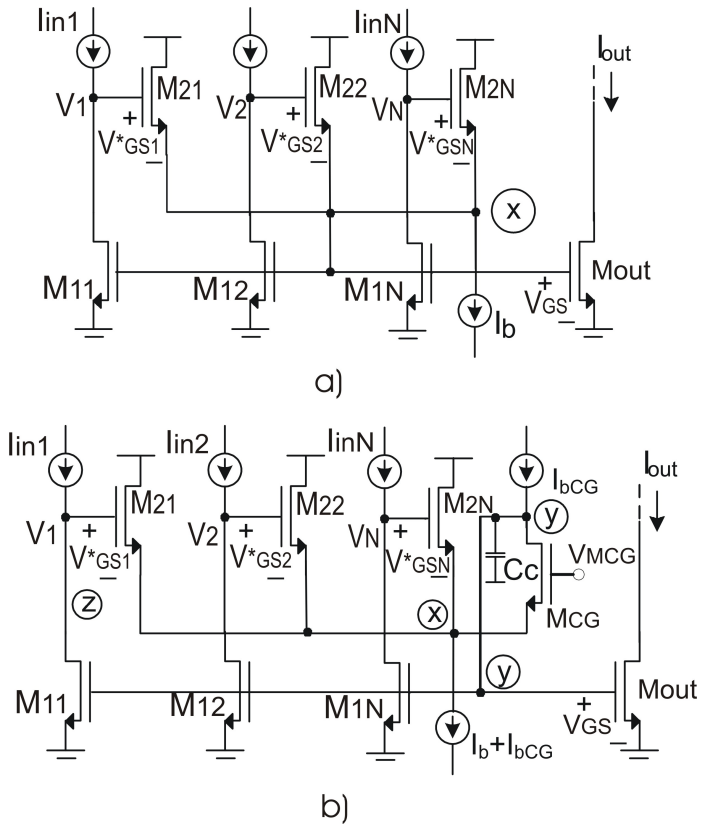

Fig. 1. a) Lazzaro's circuit with N cells. b) Proposed circuit with the improvement stage.

3.1 Stability of the proposed circuit

Each cell of the proposed circuit has three open loop poles: two common low frequency poles, p_y and p_z, and one of high frequency p_x. The dominant pole p_y has the capacitances C_{gs} of all M_{1N} transistors connected to this node plus the compensation capacitor Cc, i.e. $p_y = 1/(2\pi C_y r_{oMCG})$ and the first non-dominant pole is $p_z = 1/(2\pi C_z r_{oM1})$, where C is the total capacitance associated to a given node.

The gain bandwidth product is given by GBW $= A_o\omega_{py} \approx g_{mMCG}/C_y$, for stability the condition $\omega_{py} \geq 3$GBW must fulfill and from this we derive:

$$\frac{C_y}{C_z} \geq 3g_{m_{MCG}}r_{oMCG} \tag{2}$$

This expression was obtained neglecting the body effect term of Eq. (1). In practice a condition of $C_y/C_z \geq 500$ must be accomplished for a phase margin of $\sim 60°$. The AC PSpice simulation of the loop gain comparing the phase margin PM of a compensated and no compensated circuit is presented in Fig. 2 a).

4 Simulations and experimental results

The proposed WTA circuit was simulated using PSpice with BSIMv3.1 parameters from ON SEMI 0.5 μm CMOS technology and the transistor aspect ratio (in microns) is as follows: M1 = 5/1.5, M2 = 50/1.5, and M_{CG} = 5/5.

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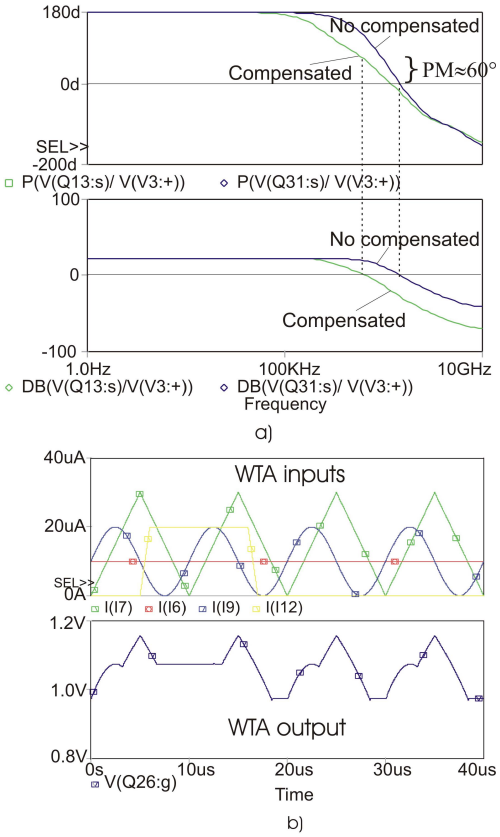

Fig. 2. a) Pspice AC simulation of the closed-loop gain, compensated and no compensated circuits. b) Transient response simulation, inputs in current mode and the output voltage response.

Since parasitic capacitance in node z is $C_z \approx 6\,\text{fF}$, the compensation capacitor in Fig. 2 b must be $Cc \approx 3\,\text{pF}$. The transient response of the circuit with four different input signals is shown in Fig. 2 b, the triangular and sinusoidal signal frequency are 100 kHz, the bias currents $I_b = 8\,\mu\text{A}$ and $I_{bCG} = 2\,\mu\text{A}$ with a $\text{V}_{\text{DD}} = 1.5\,\text{V}$ were considered. It is worth nothing that the conventional Lazzaro's circuit was not functional with voltages lower than 2.4 V.

The input currents were introduced by using a precision voltage to current converter implemented with the AD620 instrumentation amplifier. All input currents were in the range $[0, 50\,\mu\text{A}]$, as shown in Fig. 3 a, with a power supply of 1.5 V.

The measured output voltage at node "y" is shown in Fig. 3 b, the maximum frequency was 15 kHz because measurements were achieved with a larger capacitance load ($\text{C}_\text{L} > 50\,\text{pF}$) due to the probes and PCB of our setup. The microphotograph of the WTA prototype circuit is shown in Fig. 3 c.

5 Conclusions

In this work, an improvement to Lazzaro's WTA with only few extra non-common transistors was presented. This approach preserves a reduced number of transistors per cell and allows reducing the supply requirements to achieve low-voltage operation. The resolution of the original circuit was also

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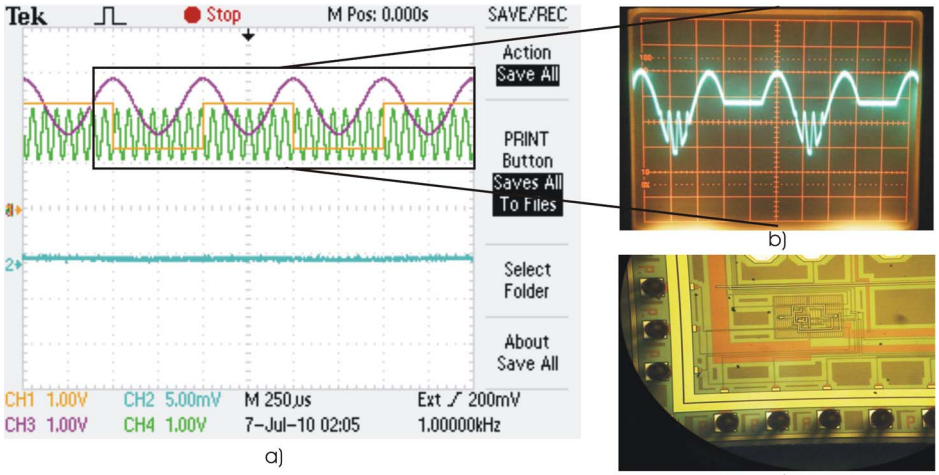

Work	Trans./cell	Tech.	V_{DD}
Lazzaro [1]	2	–	~2.5V
Donckers [2]	5	SOI 3µm	1.5V
Fish [8]	~12	CMOS 0.35µm	3.3V
Chien-Cheng [9]	>30	CMOS 0.35µm	3.3V
Baishnab [6]	5	CMOS 90nm	0.7V
This work	2	CMOS 0.5µm	1.5V

d)

Fig. 3. a) WTA inputs in current mode. b) WTA output trace, 5 mV/div, 0.2 ms/div. c) Fabricated WTA prototype, d) Comparison among other current-mode WTA/LTA circuits.

enhanced since the loop gain is increased. The stability analysis brings a minimal condition in order to guarantee a 60° phase margin. Experimental results verified the functionality of the proposed WTA with a supply of 1.5 V while the conventional Lazzaro's circuit requires a minimum supply of 2.4 V using the same technology. A detailed comparison among other circuits is presented in Fig. 3 d.

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